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FEE TRANSMITTAL
For FY 2006

☐ Applicant claims small entity status. See 37 CFR 1.27

TOTAL AMOUNT OF PAYMENT	($)	500.00

Complete if Known	
Application Number	10/663,948
Filing Date	September 16, 2003
First Named Inventor	Rajesh Tiwari et al.
Examiner Name	Phat X. Cao
Art Unit	2814
Attorney Docket No.	TI-36211

METHOD OF PAYMENT (check all that apply)

☐ Check ☐ Credit Card ☐ Money Order ☐ None ☑ Other (please identify): Deposit Account

☑ Deposit Account Deposit Account Number: 20-0668 Deposit Account Name: Texas Instruments Incorporated

For the above-identified deposit account, the Director is hereby authorized to: (check all that apply)

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FEE CALCULATION (All the fees below are due upon filing or may be subject to a surcharge.)

1. BASIC FILING, SEARCH, AND EXAMINATION FEES

	FILING FEES		SEARCH FEES		EXAMINATION FEES		
		Small Entity		Small Entity		Small Entity	
Application Type	Fee ($)	Fee ($)	Fee ($)	Fee ($)	Fee ($)	Fee ($)	Fees Paid ($)
Utility	300	150	500	250	200	100	
Design	200	100	100	50	130	65	
Plant	200	100	300	150	160	80	
Reissue	300	150	500	250	600	300	
Provisional	200	100	0	0	0	0	

2. EXCESS CLAIM FEES

Fee Description	Fee ($)	Small Entity Fee ($)
Each claim over 20 (including Reissues)	50	25
Each independent claim over 3 (including Reissues)	200	100
Multiple dependent claims	360	180

Total Claims	Extra Claims	Fee ($)	Fee Paid ($)
_____ - 20 or HP =	_____	x 50.00	= _____

HP = highest number of total claims paid for, if greater than 20.

Indep. Claims	Extra Claims	Fee ($)	Fee Paid ($)
_____ - 3 or HP =	_____	x 200.00	= _____

HP = highest number of independent claims paid for, if greater than 3.

Multiple Dependent Claims	
Fee ($)	Fee Paid ($)
_____	_____

3. APPLICATION SIZE FEE

If the specification and drawings exceed 100 sheets of paper (excluding electronically filed sequence or computer listings under 37 CFR 1.52(e)), the application size fee due is $250 ($125 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).

Total Sheets	Extra Sheets	Number of each additional 50 or fraction thereof	Fee ($)	Fee Paid ($)
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4. OTHER FEE(S)

	Fees Paid ($)
Non-English Specification, $130 fee (no small entity discount)	_____
Other (e.g., late filing surcharge): Fee for filing a Brief in support of an Appeal	500.00

SUBMITTED BY

Signature		Registration No. (Attorney/Agent) 36,981	Telephone (216) 502-0600
Name (Print/Type)	Thomas G. Eschweiler		Date 3/6/06

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TTW AFS

Docket No. TIP484US **TI-36211**

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re **PATENT** application of:

Applicant: Rajesh Tiwari et al.

Application No.: 10/663,948

For: DUAL DEPTH TRENCH TERMINATION METHOD FOR IMPROVING CU-BASED INTERCONNECT INTEGRITY

Filing Date: September 16, 2003

Examiner: Phat X. CAO

Art Unit: 2814

APPEAL BRIEF

Mail Stop Appeal Brief - Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

Applicants submit this brief in connection with the appeal of the above-identified case.

I. Real Party in Interest (37 C.F.R. § 41.37(c)(1)(i))

The real party in interest in the present appeal is Texas Instruments Incorporated.

II. Related Appeals and Interferences (37 C.F.R. § 41.37(c)(1)(ii))

Appellant, appellant's legal representatives, and/or the assignee of the present application are unaware of any appeals or interferences which will directly affect, or be directly affected by or have a bearing on the Board's decision in the pending appeal.

III. Status of Claims (37 C.F.R. § 41.37(c)(1)(iii))

Claims 1, 2, 4 and 9 are pending in the application. The rejection of claims 1, 2, 4 and 9 is appealed.

IV. Status of Amendments (37 C.F.R. § 41.37(c)(1)(iv))

Please cancel previously withdrawn claims 5-8 in order to further reduce the issues associated with this appeal. No other claim amendments have been entered subsequent to the final rejection.

V. Summary of Claimed Subject Matter (37 C.F.R. § 41.37(c)(1)(v))

As set forth in claim 1, a method for forming a copper interconnect layer is provided. A first copper region is formed over a semiconductor. (*See*, *e.g.*, page 5, lines 11-15; Fig. 2a). A low K dielectric layer is formed over the copper region. (*See*, *e.g.*, page 5, lines 14-19; page 6, lines 1-15; Fig. 2a). A plurality of vias are formed in a first region of the low K dielectric layer. (*See*, *e.g.*, page 6, lines 15-23; Fig. 2a). A trench is formed with a first edge in the low K dielectric layer over the plurality of vias wherein the trench extends a minimum length of 0.2 μm beyond the edge α of a via closest to the first edge of said trench. (*See*, *e.g.*, page 7, line 5 to page 9, line 1; Fig. 2a, Fig. 2b, and Fig. 2c). The trench and the plurality of vias are filled with copper. (*See*, *e.g.*, page 9, lines 2-8).

As set forth in claim 9, a method for forming integrated circuit copper interconnects is provided. A first copper region is formed over a semiconductor. (*See*, *e.g.*, page 5, lines 11-15; Fig. 2a). A low K dielectric layer is formed over the copper region. (*See*, *e.g.*, page 5, lines 14-19; page 6, lines 1-15; Fig. 2a). A plurality of vias are formed in a first region of the low K dielectric layer wherein the plurality of vias are separated from one another by a distance less than 1.0um. (*See*, *e.g.*, page 6, lines 15-23; page 10, lines 3-8; Fig. 2e). A trench is formed with a first edge in said low K dielectric layer with a first depth d1 in the first region and a second depth d2 at the trench edge over the plurality of vias wherein d1 is greater than d2, and the trench extends a minimum length of 0.2um beyond the edge α of a via closest to the first edge of said trench. (*See*, *e.g.*, page 7, line 5 to page 9, line 1; page 9, lines 10-21; Fig. 2c). The trench and the plurality of vias are filled with copper wherein the copper used to fill the vias contacts the first copper region. (*See*, *e.g.*, page 9, lines 2-8; Fig. 2d).

VI. Grounds of Rejection to be Reviewed on Appeal (37 C.F.R. § 41.37(c)(1)(vi))

Claims 1, 2, 4 and 9 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 6,433,432 (Shimuzu) in view of U.S. Patent Application No. 10/454,667, Publication No. 2003/0227089 (Watanabe et al.).

VII. Argument (37 C.F.R. § 41.37(c)(1)(vii))

A. REJECTION OF CLAIMS 1, 2, 4 AND 9 UNDER 35 U.S.C. § 103(a)

Claims 1, 2, 4 and 9 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 6,433,432 (Shimuzu) in view of U.S. Patent Application No. 10/454,667, Publication No. 2003/0227089 (Watanabe et al.). Reversal of the rejection is respectfully requested for at least the following reasons.

To establish a *prima* facie case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations.

The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, not in applicant's disclosure. In re Vaeck, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991).

The cited references fail to teach or suggest all of the claim limitations of claims 1-2, 4 and 9 for at least the reasons below and, therefore, a prima facie case of obviousness has not been established and this rejection should be reversed. Applicants show *infra* that Shimuzu fails to require a *minimum* length between the trench edge and the closest via edge and that Watanebe et al. fail to cure this deficiency of Shimuzu.

Claim 1 includes forming a trench with a first edge in said low K dielectric layer over said plurality of vias wherein said trench extends *a minimum length* of 0.2 μm beyond the edge α of a via closest to the first edge of said trench, which is not taught or suggested by the cited references.

Generally, Shimuzu discloses a semiconductor device having a fluorine insulating film and reduced fluorine at interconnection interfaces. The device allegedly prevents the problem of plugs being peeled off from an upper surface of the wiring layer after the protection insulating film is formed. The device of Shimuzu maintains a good connection (adhesion) between a metal film buried in a trench of a fluorine containing insulating film and another metal film connected to such metal film. (Column 2, lines 19-24). Shimuzu attempts to reduce the amount of fluorine on the surface of the metal film buried in the trench so as to improve the adhesiveness between the metal film and the metal plugs or the metal film and the overlying fluorine-noncontaining insulating film. (Column 2, lines 43-50)

The Office Action of September 9, 2005 erroneously relies upon item 12b of Shimuzu to teach the minimum length between the trench edge and the closest via, as recited in claim 1. Item 12b of Shimuzu is a pad trench 12b formed in an upper area of a second SiOF film 12, formed by patterning the second SiOF film 12. (Column 5, lines 37-41). It is conceded that Shimuzu does show a distance from an outer edge of the pad trench 12b to a via 12a, but the distance is incidental and not teaching is provided that the distance must exceed some predetermined value as recited in claim 1.

The Office Action of September 9 also erroneously asserts that Shimuzu teaches such a minimum length so as to participate in preventing peeling-off of plugs from metal wirings. It is respectfully submitted that such assertion is incorrect. Shimuzu employs a sputter to etch the surface of the copper wiring 10 *via* the holes 12a *to remove an oxide film* formed on the surface of the copper wiring 10. (Column 5, lines 45 to 48). As a result of the sputter, shoulder portions of the second SiOF film 12 around the holes 12a are obliquely scraped off to expand a diameter of the holes 12a in the neighborhood of the pad trench 12b. (Column 5, lines 49-52). ***The oblique scraping of the shoulder portions is merely a result of the sputter etch to remove the oxide film from the***

surface of the copper wiring. Shimuzu does not teach or suggest that the obliquely scraped shoulder portions participate in adhering the metal plugs. Instead, Shimuzu clearly states that the peeling off of the copper wiring 10 is prevented by sputtering of the copper wiring 10 and then exposing to the ammonia plasma or polishing the copper film 10 using a slurry after the copper wiring is formed. (Column 8, lines 43-53). Therefore, Shimuzu does not need a minimum distance from a trench edge to a via edge in order to form a shoulder portion. Accordingly, a minimum length from the trench edge to the via edge is not taught by Shimuzu expressly or inherently as recited in claim 1.

The Office Action of September 9 is apparently assuming that a shoulder portion between the closest hole and edge of the pad trench 12b is required thereby establishing a minimum distance. However, this is not the case. For example, if an edge of the pad trench 12b and an edge of the closest hole were in line with no distance or length between, there would simply be no shoulder portion to be scraped. Shimuzu does not preclude this event nor require a shoulder portion to be present between the closest hole and the edge of the pad trench 12b. As stated above, Shimuzu scrapes the shoulders only as a result of removing the oxide film from the surface of the copper wiring. As a result, Shimuzu does not require or teach a minimum distance, such as the minimum length of 0.2 μm, between an edge of the pad trench and an edge of the closest hole as claimed.

The Advisory Action of November 28 simply dismisses Applicant's above argument by suggesting that Figs. 3H and 3I of Shimuzu include a scraping portion and a planar portion formed between the trench edge and the via edge. Figs. 3H and 3I of Shimuzu *do suggest a distance between a trench edge and an edge of a via*, but this is not sufficient to teach *a method of forming a copper interconnect layer including forming a trench that extends a minimum length of 0.2 μm beyond the edge α of a via closest to the first edge of said trench as* in claim 1.

It is noted that the Office Action of September 9 suggests that the scraping off of the shoulders participates in preventing the peeling off of the plugs from the metal wirings. Applicants respectfully disagree. As shown above, Shimuzu relies on

adheshion between the copper wiring and the overlying plugs and film in order to prevent peeling. The sputter is performed to remove fluorine from the surface of the copper wiring 10 and the shoulder formation is merely an unintended by-product thereof. (Column 8, lines 43-53, and, for example Figs. 5, 6, 12, and 13). Therefore Shimuzu fails to teach or suggest the above highlighted feature.

Watanebe et al. fail to cure the *deficiencies* of Shimuzu.

The Office Action of September 9 suggests that Watanabe et al. teach a minimum length, however, it does not. Watanabe et al. merely provide dimension examples of various wiring patterns and width patterns (Paragraph 175) and does not teach or suggest a *minimum* length between a via edge and a trench edge.

Claims 2 and 4 depend from claim 1 and are, therefore, not taught by Shimuzu and Watanabe et al., alone or in combination, for the above reasons. Additionally, claim 9 also recites the minimum length between the trench edge and the closest via and is also not taught by Shimuzu and Watanabe et al., alone or in combination, for the above reasons.

Therefore claims 1, 2, 4 and 9 are non-obvious over the cited art. Accordingly, withdrawal of the rejection of claims 1, 2, 4 and 9 is requested.

CONCLUSION

For at least the above reasons, the claims currently under consideration are believed to be patentable over the cited references. Accordingly, it is respectfully requested that the rejections of the pending claims be reversed.

For any extra fees or any underpayment of fees for filing of this Brief, the Commissioner is hereby authorized to charge the Deposit Account Number 20-0668, TIJ-30686.

Respectfully submitted,
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CERTIFICATE OF MAILING (37 CFR 1.8a)

I hereby certify that this paper (along with any paper referred to as being attached or enclosed) is being deposited with the United States Postal Service on the date shown below with sufficient postage as first class mail in an envelope addressed to: Mail Stop Appeal Brief - Patents, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

Date: March 6, 2006

Christine Gillroy

VIII. Claims Appendix (37 C.F.R. § 41.37(c)(1)(viii))

1. (Previously Presented) A method for forming a copper interconnect layer, comprising:

forming a first copper region over a semiconductor;

forming a low K dielectric layer over said copper region;

forming a plurality of vias in a first region of said low K dielectric layer;

forming a trench with a first edge in said low K dielectric layer over said plurality of vias wherein said trench extends a minimum length of 0.2 μm beyond the edge α of a via closest to the first edge of said trench; and

filling said trench and said plurality of vias with copper.

2. (Original) The method of claim 1 wherein said trench is formed with a first depth d1 in said first region and a second depth d2 at said trench edge wherein d1 is greater than d2.

Claim 3 (Canceled)

4. (Previously Presented) The method of claim 1 wherein said plurality of vias are separated by a distance less than 1.0um.

Claims 5-8 (Cancelled)

9. (Original) A method for forming integrated circuit copper interconnects, comprising:

forming a first copper region over a semiconductor;

forming a low K dielectric layer over said copper region;

forming a plurality of vias in a first region of said low K dielectric layer wherein said plurality of vias are separated by a distance less than 1.0um;

forming a trench with a first edge in said low K dielectric layer with a first depth d1 in said first region and a second depth d2 at said trench edge over said plurality of vias wherein d1 is greater than d2, and said trench extends a minimum length of 0.2um beyond the edge α of a via closest to the first edge of said trench; and

filling said trench and said plurality of vias with copper wherein said copper used to fill said vias contacts said first copper region.1. (Previously presented) A method for cleaning a photoresist or an organic substance from a semiconductor wafer, consisting essentially of:

generating vapor by heating ultrapure water;

increasing the number of hydroxyl radicals in the vapor by irradiating ultraviolet rays into the vapor; and

removing an organic substance from said semiconductor wafer surface by blowing the vapor at a temperature of 85°C or higher onto the semiconductor wafer surface.

IX. Evidence Appendix (37 C.F.R. § 41.37(c)(1)(ix))

No additional evidence not already part of the official record is relied upon in the arguments provided herein.

X. Related Proceedings Appendix (37 C.F.R. § 41.37(c)(1)(x))

Not applicable.